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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,304	09/16/2003	Kallol Bera	8477/ETCH/DRIE	1356

55649 7590 06/01/2006

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EXAMINER

PHAM, THANH V

ART UNIT PAPER NUMBER

2823

DATE MAILED: 06/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/663,304

Applicant(s)

BERA ET AL.

Examiner

Thanh V. Pham

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 23 May 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-17 and 40-45 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-17 and 40-45 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Response to Amendment*

#### *Drawings*

1. Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (*instant specification's [0030] indicates it as CENTURA® system*). See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

#### *Claim Rejections - 35 USC § 103*

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-6, 8-10 and 40-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. US 6,797,633 B2 in combination with Ma et al. US 2004/0161930 A1 and/or Ikeda US 6,426,299 B1.

*Re claim 1 and 40, the Jiang et al. reference discloses a method of fabricating an interconnect structure, which "may be the first or any subsequent metal interconnect level of the semiconductor device 120" (col. 3, lines 24-26), comprising:*

(a) providing (first metal interconnect level of the semiconductor device 120 being formed) a substrate 100 having a film stack comprising sequentially formed on the substrate a first barrier layer 101, a conductive layer 124 embedded in a first dielectric layer 102/104, (subsequent metal interconnect level of the semiconductor device 120 being formed) a second barrier layer 101, a second dielectric layer 102/104, and a cap layer 105 (fig. 1A, without substrate 100, laying on top of fig. 1F);

(b) etching a via hole 106 in the cap layer and the second dielectric layer 102/104 (fig. 1C);

(c) filling a portion of a depth of the via hole with a masking material 107 (fig 1D);

(d) etching in-situ the cap layer 105, a trench 108 in the second dielectric layer 102/104, the masking material 107, and the second barrier layer 101 (figs. 1E and 1F);  
and

(e) metallizing the via hole and the trench (fig. 1F).

The Jiang et al. reference discloses substantially all of the steps of the instant invention, teaches O<sub>2</sub> plasma and other chemistries are provided with or without inert gases to treat low-k films without damage to the OSG film but remove the resist (col. 3, lines 45-67) “[t]he exposure energy required to clear resist inside a via is the lowest for the wafer with in-situ O<sub>2</sub> plasma ash, indicating the most robustness for fighting poisoning” (col. 4, lines 15-26).

The Jiang et al. reference lacks providing a plasma source power of at least about 1000 Watts and a bias power of at least about 800 Watts *while etching* during at least a portion of the etching period *or while etching the dielectric layer*.

The Ma et al. reference discloses in-situ discharge to avoid arcing during plasma etch method wherein a substrate is fastened to a chuck in a process chamber (abstract), an inert gas and an etching gas are flowed into the chamber during the etching sequence (figs. 2-5) wherein the power is between 100 and 1000 Watts while chamber pressure is held between 20 and 150 mTorr [0028], a fluorocarbon gas  $C_xF_yH_z$  where x and y are integers equal or greater than 1 and z is either 0 or an integer equal or greater than 1; the flow rate of fluorocarbon gas is between 0 and 50 sccm may be combined with  $N_2$  and other fluorocarbon gas, the flow rate of the additional gas is also from 0 to 50 sccm, the same RF power, chamber pressure and time period apply in one step as in the other previous step [0029], the choice of gas for the discharge may be a matter of convenience [0033].

And the Ikeda reference discloses a method of etching the structure of fig.3 wherein a SiON 103, a  $SiO_2$  104, an organic ARC 105 and a photoresist pattern 106 formed in that sequence on the base 101 with plug 102 embedded to reduce the F radicals (col. 1, lines 28-29 and col. 2, lines 35-37). The method in fig. 4 discloses plasma source power of at least about 1000 Watts and a bias power of at least about 800 Watts while etching during at least a portion of etching period and/or while etching a dielectric layer (step II, e.g.).

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the sub-steps of Jiang et al. with the power, pressure and flow rates as taught by Ma et al. and/or Ikeda *to provide a plasma source power of at least about 1000 Watts* (both in Ma et al. and Ikeda) *and a bias power of at least about 800 Watts*

(in Ikeda) while etching *during at least a portion of etching period according to the choice of gas as suggested by Ma et al.* and/or Ikeda because the power, pressure and flow rates as suggested/taught by Ma et al. and/or Ikeda would provide the sub-steps of Jiang et al. with in-situ discharge to avoid arcing during plasma etch processes and to reduce the F radicals which form a hardened surface layer.

*Re claim 2*, the Jiang et al. reference teaches wherein the cap layer comprises  $\text{SiO}_x\text{N}_y$ , where x and y are integers (col. 3, line 40).

*Re claims 3 and 41*, the Jiang et al. reference teaches wherein the first dielectric layer and the second dielectric layer comprise at least one of carbon doped silicon oxide, organic doped silicon glass, and fluorine doped silicon glass (col. 3, lines 28-36).

*Re claim 4*, the Jiang et al. reference teaches wherein the first barrier layer and the second barrier layer comprise at least one of  $\text{SiO}_2$ , SiC and  $\text{Si}_3\text{N}_4$  (col. 1, line 52).

*Re claim 5*, the Jiang et al. reference teaches wherein the conductive layer comprises at least one of Cu, Al, Ta, W, Ti, TaN and TiN (col. 2, line 41).

*Re claim 6*, the Jiang et al. reference teaches wherein the masking material is selected from a group consisting of an organic material and photoresist (col. 4, lines 9-14).

*Re claim 8*, the Jiang et al. reference teaches wherein the step (c) further comprises: applying the masking material 107 to the substrate to fill the via hole 106; and etching back the masking material 107 until the masking material is

removed from the via hole to a pre-determined depth that is smaller than a depth of the trench (col. 4, lines 9-15).

*Re claims 9 and 42-43*, the Jiang et al. reference teaches wherein the etching step further comprises: providing O<sub>2</sub> at a flow rate from about 100 to 1000 sccm; maintaining a chamber pressure at about 5 to 200 mTorr; and applying a cathode bias power between 100 and 400 W (col. 3, lines 1-4).

*Re claim 10*, the Jiang et al. reference teaches wherein the step (d) further comprises: forming on the cap layer a second patterned etch mask 132 to define the trench 108; and stripping the second patterned etch mask 132 contemporaneously with etching the masking material (col. 4, lines 27-30).

4. Claims 7 and 11-17, 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. in combination with Ma et al. and/or Ikeda as applied to claims 1-6, 8-10 and 40-43 above, and further in view of Chun et al. TW 544815 A and Samukawa et al. US 6,177,146 B1.

Although the Jiang et al. reference discloses in the step (b): forming a first patterned etch mask 130 on the cap layer 105 to defined via hole 106; etching the via hole; and stripping the first patterned etch mask (figs. 1C and 1D), *re claim 7*; and in step (d): “[t]rench pattern 132 and BARC 107 are then removed. The capping layer 105 and etchstop layer 101 are removed next during and etchstop etch” (col. 4, lines 28-30) without details of VHF frequency, bias power at a frequency, or source power and the ratio of CF<sub>4</sub>:N<sub>2</sub> in each sub-step, *re claims 11-17 and 44-45*. The combination teaches substantially all of the instant invention, the combination still lacks the ratio of CF<sub>4</sub>:N<sub>2</sub> in

a range from 1:1 to 1:5 in forming the via hole and an indication of the frequency of the VHF while etching.

The Chun et al. reference teaches etching through a cap layer on the dielectric layer using N<sub>2</sub> and CF<sub>4</sub> in the ratio of 0-10:1.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the via hole etching of the combination with the ratio of CF<sub>4</sub>:N<sub>2</sub> as taught by Chun et al. because that ratio of Chun et al. would improve the etching rate of nitride to oxide layer as taught by Jiang et al.

Samukawa et al. teaches that etching by exposing to plasma has been widely applied since it is highly practicable. High-density plasma etching generated in the course of electric discharge caused by applying an electric field of high frequency ranging in VHF to UHF bands, nearly from 100 to 1,000 MHz (col. 1, lines 20-47).

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the process of the combination with an appropriate VHF frequency as taught by Samukawa et al. because the frequency of Samukawa et al. would provide the method of the combination with highly practicable. The use of frequency ranging in VHF to UHF bands in plasma etching is well known to those skill in the art as taught by Samukawa et al.

***Response to Arguments***

5. Applicant's arguments filed 05/23/2006 have been fully considered but they are not persuasive.

6. Applicant argue that Fig. 3 is not prior art because "the examiner is mistaken" based on the reading of paragraph [0044]. The examiner does not agree. Paragraph [0044] is quoted without changing a word to show the admitted prior art

[0044] FIG. 3 depicts a schematic diagram of the etch reactor 302 that illustratively may be used to practice portions of the invention. The etch reactor is generally used as a processing module of the CENTURA® semiconductor wafer processing system available from Applied Materials, Inc. of Santa Clara, California.

7. Applicant's argument about the discharge sequence of the Ma et al. reference on page 7 of the Remark is irrelevant because this parameter is not recited in the rejected claim(s).

8. It is agreed that the Jiang et al. reference lacks providing a plasma source power of at least about 1000 Watts and a bias power of at least about 800 Watts *while etching* during at least a portion of the etching period *or while etching the dielectric layer* and the Ma et al. reference "is silent regarding the bias power applied" (Remark's page 7). However, Ma et al. "discloses applying an RF power in the range of 100 to 1000 Watts for a 200 mm wafer and from 100 to 2000 Watts for a 300 mm wafer (the same page 7) and the Ikeda reference discloses in fig. 4 plasma source power of at least about 1000 Watts and a bias power of at least about 800 Watts *while etching* during at least a portion of etching period and/or *while etching a dielectric layer*, step II, e.g. (not as alleged as in Remark's page 9).

9. In response to applicant's argument that there is no suggestion to combine the references (Remark's page 9), the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the Jiang reference teaches substantially all of the claimed invention lacks providing a plasma source power of at least about 1000 Watts and a bias power of at least about 800 Watts *while etching*; therefore, *Ma et al.* and/or Ikeda are used to modify/combine because the power, pressure and flow rates as suggested/taught by *Ma et al.* and/or Ikeda would provide the sub-steps of Jiang et al. with in-situ discharge to avoid arcing during plasma etch processes and to reduce the F radicals which form a hardened surface layer as stated above. (*Ma's* abstract: "the method is extendable to etching low K dielectric layers" and "different mechanism to reduce F radicals in the process chamber" of Ikeda as recognized by applicant does not negate the provided step II (e.g.) in Ikeda's fig. 4).

10. In response to applicant's argument on pages 10-11 that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made,

and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). The instant claimed invention is the combination of many etching steps onto many different layers for a dual damascene interconnection structure formation. The examiner takes initial burden to analyze the claim and applies prior art to each steps in the instant claimed invention. The objective teachings of prior art go along with many steps in the combination. The reasons for the combinations are stated. The tests for obviousness are also provide. The references when combined would teach the limitations recited in the claims.

11. In response to applicant's argument that the different mechanism of Ideka is not a good reason for the combination, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

12. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). ). In this instant neither Ma nor Chun nor Samukawa is used for the bias power, Ikeda is.

13. The rejections are maintained as in the above.

***Conclusion***

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-Th (6:30-5:00).

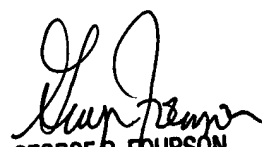
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2823

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TWP

05/25/2006

  
GEORGE R. FOURSON  
PRIMARY EXAMINER